We Claim:

1. A sense amplifier configuration for a memory device having a memory area including a plurality of memory elements having a memory state and further including access line devices having at least one of bit line devices and word line devices for addressing the memory elements, the sense amplifier comprising:

an input area configured to be connected during operation to at least a selected one of the access line devices for selected memory elements in the memory area in order to ascertain the memory state for at least one of the selected memory elements;

an output area outputting during operation an output signal representing the ascertained memory state;

a compensation voltage source device configured to control a voltage applied to the selected access line device in relation to an unselected memory area during operation; and

a compensation current source device generating an electric compensation current during operation and supplying the electric compensation current to at least one of the access line devices, a time profile of the compensation current being chosen to generate a constant potential difference over time

and during operation in interaction with said compensation voltage source device on the selected access line device relative the unselected memory area.

2. The sense amplifier configuration according to claim 1, wherein the memory cell configuration being read includes MRAM cells.

3. The sense amplifier configuration according to claim 1, wherein the memory area in the memory device is read using an electric current flowing through the selected memory elements.

4. The sense amplifier configuration according to claim 3, wherein the selected memory elements are memory cells.

5. The sense amplifier configuration according to claim 1, wherein the output signal is output as an electric current.

6. The sense amplifier configuration according to claim 1, wherein said compensation voltage source device has first and second input connections, first and second output connections, and an inverting amplifier device.

7. The sense amplifier configuration according to claim 6, wherein said inverting amplifier device is an operational amplifier.

8. The sense amplifier configuration according to claim 7, wherein:

said operational amplifier device has a noninverting input and an inverting input; and

said first and second input connections of said compensation voltage source device are connected firstly to said noninverting input and said inverting input of said operational amplifier device and secondly via said input area to a potential.

9. The sense amplifier configuration according to claim 8, wherein the potential is a deactivation potential.

10. The sense amplifier configuration according to claim 8, wherein the potential is an equalization potential.

11. The sense amplifier configuration according to claim 8, wherein the potential is of the unselected memory area (2').

12. The sense amplifier configuration according to claim 8, wherein the potential is at least of a given one of the access line devices corresponding to the unselected memory area (2').

13. The sense amplifier configuration according to claim 8, wherein the voltage is of a system of unselected ones of the word lines.

14. The sense amplifier configuration according to claim 8, wherein the voltage is of the selected memory elements provided via the selected and connected one of the access line devices.

15. The sense amplifier configuration according to claim 7, wherein:

said operational amplifier device has an output; and

one of said output connections of said compensation voltage source device connects to said output of said operational amplifier device.

16. The sense amplifier configuration according to claim 15, wherein said one of said output connections of said compensation voltage source device connects to said output of said operation amplifier device via the selected and connected access line device to the selected memory element to allow the potential difference between the unselected memory area and the selected, connected access line device to be controlled by feedback.

17. The sense amplifier configuration according to claim 16, wherein the potential difference is constant over time.

18. The sense amplifier configuration according to claim 6, wherein said compensation current source device has a connection connecting said compensation current source device to the selected, connected access line device, in order to supply a compensation current at least in part to the selected, connected access line device during operation.

19. The sense amplifier configuration according to claim 18, wherein the selected, connected access line device is a selected, connected bit line device.

20. The sense amplifier configuration according to claim 18, wherein said connection connects said compensation current source device to said second input connection and said second output connection of said compensation voltage source device.

21. The sense amplifier configuration according to claim 1, wherein said compensation current source device provides a compensation current having a value at least equaling an electric current offset corresponding to the voltage offset in said compensation voltage source device via a resistive network of the memory elements in the entire memory area, the compensation current (Icomp) satisfying a relationship

$$Icomp \geq \frac{Vos}{Rpar' \| Rc} = \frac{Vos}{Rpar},$$

where Rpar signifies a nonreactive resistance of the entire memory area and is represented as a parallel circuit including a nonreactive resistance Rpar' of the unselected memory area and a nonreactive resistance Rc of the selected memory elements.

22. The sense amplifier configuration according to claim 21, wherein said compensation current source device self-calibrates during operation in order to best approximate a value for the compensation current corresponding to

$$\frac{Vos}{Rpar' \| Rc} = \frac{Vos}{Rpar}.$$

23. The sense amplifier configuration according to claim 1, further comprising an amplifier device disposed between said input area and said output area; said amplifier device receiving during operation an input signal representing the memory state of the selected and connected memory element via said input area, generating an amplified signal from the input signal, and outputting the amplified signal via said output area.

24. The sense amplifier configuration according to claim 23, wherein said amplifier device is a current amplifier device.

25. The sense amplifier configuration according to claim 23, wherein said amplifier device has an input connection configured to be connected during operation to said input area.

26. The sense amplifier configuration according to claim 25, wherein said input connection of said amplifier device is connected to the selected, connected access line device.

27. The sense amplifier configuration according to claim 26, wherein the selected, connected access line device is a selected, connected bit line device.

28. The sense amplifier configuration according to claim 26, wherein said input connection of said amplifier device is connected to said compensation current source device (30).

29. The sense amplifier configuration according to claim 25, wherein said amplifier device has an output connection configured to be connected during operation to said output area.

30. The sense amplifier configuration according to claim 25, wherein said amplifier device has two transistor devices having source, drain and gate regions, said source regions of said two transistor devices are connected to one another, and said gate regions of said transistors are connected, and said drain regions of said transistor devices are connected to said input connection and said output connection of said amplifier device.

31. The sense amplifier configuration according to claim 30, wherein said two transistor devices are MOSFETs.

32. The sense amplifier configuration according to claim 30, wherein said amplifier device has a second input connection connected to said gate regions of said transistor devices.

33. The sense amplifier configuration according to claim 29, further comprising a calibration device configured to equalize at least one of an excess compensation current and an excess output signal from said amplifier device during operation and having alternately activatable current storage and current release functions.

34. The sense amplifier configuration according to claim 33, wherein said calibration device is disposed between said

output connection of said amplifier device and said output area.

35. The sense amplifier configuration according to claim 34, wherein said calibration device has an input connection connected to said output connection of said amplifier device and a first output connection connected to said output area.

36. The sense amplifier configuration according to claim 33, wherein said calibration device has a second output connection connected to said compensation current source device.

37. The sense amplifier configuration according to claim 33, wherein said calibration device has a current storage device performing the current storage and the current release functions.

38. The sense amplifier configuration according to claim 37, wherein said current storage device is configured to store at least one of an excess compensation current and an excess output signal during operation before a reading state and to supply the at least one of an excess compensation current and an excess output signal during the reading state.

39. The sense amplifier configuration according to claim 38, wherein said current storage device stores the excess

compensation current from said compensation current source device before the reading state and supplies the excess compensation current to said compensation current source device during the reading state.

40. The sense amplifier configuration according to claim 38, wherein said current storage device stores the excess output signal from said amplifier device before the reading state and supplies the excess output signal to said amplifier device during the reading state.

41. The sense amplifier configuration according to claim 37, wherein said current storage device is a transistor device.

42. The sense amplifier configuration according to claim 41, wherein said transistor device is a MOSFET.

43. The sense amplifier configuration according to claim 37, wherein said current storage device includes a transistor device.

44. The sense amplifier configuration according to claim 42, wherein:

said calibration device has an input connection and an output connection; and

said transistor device has a drain region and a source region;

said drain region is connected to said input connection of said calibration device; and

said source region is connected to said compensation current source device via said output connection of said calibration device.

45. The sense amplifier configuration according to claim 44, wherein said current storage device has a switching device connecting and isolating said gate region of said transistor device in said current storage device and said drain region before and during a reading state, to allow a gate capacitor in said gate region of said transistor device to be switched as a current storage element.

46. The sense amplifier configuration according to claim 33, wherein said calibration device has an input connection, an output connection, and a further switching device configured to make a direct electrical connection between said input connection and said output connection of said calibration device during a reading state and can break said direct electrical connection before a reading state.